UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,830	04/16/2004	Sheng Teng Hsu	SLA0871	9432

55376 7590 02/23/2006

ROBERT D. VARITZ
4915 S.E. 33RD PLACE
PORTLAND, OR 97202

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,830	HSU, SHENG TENG	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004 and 10 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☑ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 04/16/2004 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention II, claims 10-24, in the reply filed on 08/10/2005 is acknowledged.

3. Claims 1-9 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 08/10/2005, as noted above.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figs. 4-5, middle electrodes 14 – which should be **18**; middle electrode 14 of the second memory level – which should be **38**. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s)

should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following typographical errors and informalities: page 5, line 25, "middle electrode 34", which should be "middle electrode **38**"; page 1, line 9, Application Serial No. "10/794,308", which should be "10/794,309", and "now Patent 6,925,001" should be added, following the serial number. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 10-12, 14-17, and 19-21** are rejected under 35 U.S.C. §103(a) as being unpatentable over Rinerson et al. U.S. Patent Application Publication 20040159828 (the '828 reference).

The '828 reference discloses in the figures and respective portions of the specification a method of manufacturing a memory structure substantially as claimed.

Specifically, the '828 reference discloses in Figs 13-14 and respective portions of the specification a method of manufacturing a memory structure comprising steps a-f as claimed in claim 10, or in other words, discloses steps for forming a first-level memory array of a multiple-level memory structure or a single-level memory array of a memory structure; and discloses in Fig. 4 and respective portions of the specification a multiple-level memory structure. Therefore, it can not be said that the reference discloses exactly all steps as recited in claim 10, which amount to forming a multiple-level memory structure.

More specifically and with reference to **claim 10**, the reference discloses a method of manufacturing a memory structure comprising the steps of:

a) providing a substrate (1110/1115/1120, or 1110, Fig. 13);

b) depositing and planarizing a silicon oxide layer (1105, paragraph [0100], "SiO_2") overlying the substrate;

c) depositing electrode material (1305, paragraph [0102]) over the silicon oxide layer;

d) depositing resistive memory material (1310, paragraph [0103]), and a second electrode material (1315) overlying the electrode material;

e) patterning the second electrode material and the resistive memory material, stopping at the electrode material (paragraph [0103]);

f) patterning the electrode material to form electrodes having a first orientation; and

g') depositing silicon oxide (1405, Fig. 14, paragraph [0104]) and planarizing the silicon oxide.

However, the reference does not further teach **(10a)** said planarizing the silicon oxide in step g' is planarizing the silicon oxide stopping at the second electrode material; instead, the

reference discloses planarizing the silicon oxide stopping at the conductive plug 1425 which is connected to the second electrode material (Fig. 14); and further does not teach **(10b)**:

h) depositing a electrode material; and

i) repeating steps (d) through (g), wherein step (f) patterning the electrode material forms electrodes at a second orientation, whereby a first two layer resistive memory array is formed.

Nevertheless, as for **(10b)**, which amounts to steps h and i as claimed, in order to form the multiple-level memory structure as depicted in Fig. 4, it would necessitate:

h) depositing an electrode material (to form y-direction conductive line 440, Fig. 4, paragraph [0037]); and

i) repeating steps (d) through (g), wherein step (f) patterning the electrode material forms electrodes at a second orientation, whereby a first two layer (generally indicated at 405 and 410, Fig. 4, paragraph [0037]) resistive memory array is formed.

As for **(10a)**, it is clear from Fig. 4 that the memory structure does not call for conductive plug 1425; therefore, the process as detailed for forming the structure of Figs. 14-15, modified to form the structure of Fig. 4, would amount to g) depositing silicon oxide (1405) and planarizing the silicon oxide stopping at the second electrode material, as claimed. Furthermore, the reference teaches in paragraph [0044] that each of memory plug 305 or 610 (Fig. 3), or 405 or 410 (Fig. 4), or the structure generally indicated by 1305/1310/1315/1425 (Fig. 14, which, as detailed above, electrode/memory material/electrode/via plug), could contain "any other materials that may be desirable for fabrication or functionality". In other words, the reference appears to teach that the extra via plug 1425 of Fig. 14 is not required, the more clearly describing the teachings of Fig. 4.

Referring to **claim 11**, the reference further discloses repeating steps (b) through (i) to form a second two layer (generally indicated at 415, 420) resistive memory array above the first two layer resistive memory array.

Referring to **claim 14**, the reference further discloses that the electrode material is platinum or iridium (paragraph [0102] and [0046]-[0060]).

Referring to **claims 15-17**, the reference further discloses that the resistive memory material is a perovskite material (paragraph [0073]), that the perovskite material is PCMO (paragraph [0073]), and that the perovskite PCMO material is a colossal magnetoresistance (CMR) material (by definition in the art. See, for example, Ignatiev et al., U.S. 6,473,332, which is cited by Applicant, Abstract and col. 8).

Referring to **claim 19**, the reference further discloses that the step of planarizing the silicon oxide in step (g) or (g') comprises chemical mechanical polishing (paragraph [0100]).

Referring to **claim 20**, the reference further discloses that first orientation and the second orientation produce electrodes arranged as a cross-point array (best seen in Fig. 4).

Referring to **claim 21**, the reference further discloses forming peripheral circuitry prior to step (a) (Figs. 13-14).

Referring to **claim 12**, although the reference does not disclose a range of thickness for the silicon oxide layer as claimed, since the criticality of the range of thickness has not been established, choosing such a range of thickness would have been obvious to one of ordinary skill in the art at the time the invention was made.

7. **Claims 13 and 18** are rejected under 35 U.S.C. §103(a) as being unpatentable over Rinerson et al. U.S. Patent Application Publication 20040159828 (the '828 reference) as applied above for claims 10 and 16 and further in view of Ignatiev et al. U.S. 6,473,332 (the '332 reference, which is cited by Applicant).

The '828 reference discloses a method of manufacturing a memory structure substantially as claimed and as detailed above for claims 10 and 16, including the electrode layer formed of, for example, IrO_2 , and the memory layer formed of a perovskite material, for example, PCMO, but does not disclose materials as claimed.

The '332 reference, in also disclosing a memory structure, discloses IrO_2 and the claimed material for the electrode layer (col. 7, lines 10-17 and col. 8, lines 14-31), thereby teaching that the materials are art-equivalent; and discloses PCMO and the claimed material for the perovskite-material memory layer (col. 7, lines 17-23), thereby teaching that the materials are art-equivalent.

8. **Claims 22-24** are rejected under 35 U.S.C. §103(a) as being unpatentable over Rinerson et al. U.S. Patent Application Publication 20040159828 (the '828 reference) as applied above for claim 11 and further in view of in view of Rinerson et al. U.S. Patent Application Publication 20040160820 (the '820 reference).

The '828 reference discloses a method of manufacturing a memory structure substantially as claimed and as detailed above for claim 11, including forming a second two layer resistive memory array above the first two layer resistive memory array but does not disclose forming vias to connect at least one electrode from the second two layer resistive memory array to at

least one electrode from the first two layer resistive memory array. The '828 reference thus further does not disclose that the connected electrodes form a common bit line or a common word line.

The '820 reference, in also disclosing a memory structure including forming a second two layer resistive memory array (415,420, Figs. 4, 10; 2415, 2420, ..2440, Fig. 24; paragraph [0082]) above a first two layer resistive memory array (405, 410, Figs. 4, 10; 2405, 2410, Fig. 24), teaches forming vias ("thru" 510, Figs. 5, 10, thru's 2470, 2475, Fig. 24) to connect at least one electrode from the second two layer resistive memory array to at least one electrode from the first two layer resistive memory array (Figs. 4-5, 10, and 24) to enable sharing driver or decoding logic (paragraphs [0100] and [0128]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '828 reference's device such that forming the memory structure includes connecting at least one electrode from the second two layer resistive memory array to at least one electrode from the first two layer resistive memory array. One would have been motivated to make such a change in view of the teachings in the '820 reference that such a change enables sharing driver or decoding logic. The connected-together electrodes, or common electrode in other words, having said first and second directions (x and y directions) are also known as connected-together bit line or word line, or common bit line or word line, as such terms are used in the art.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
February 16, 2006